DELKIN DEVICES®

C670 Series

Ultra High Performance CompactFlash

Engineering Specification

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1.0 Product Overview

Delkin Devices' *Ultra High Performance CompactFlash* memory cards possess advanced features for applications requiring high performance and large storage capacity. These cards have superior features such as:

- Global Wear Leveling
- Advanced ECC error correction 72 bit / 1KB
- Up to 150 MB/sec sustained read speed and 135 MB/sec sustained write speed*
- Operating Temperature Range: SLC Industrial & MLC Industrial (-40 to 85˚C)
- Compliant with CompactFlash Specification Rev. 6.0, Type 1, and ATA/ATAPI-8
- Operating modes – PIO Mode 0 – 6, Multiword DMA Mode 0 – 4, Ultra DMA Model 0 – 7, PCMCIA Ultra DMA Mode 0 - 7
- Compliant with European Union Directive 2011/65/EU (ROHS 2-2.4) and GB/T 26572-2011 (China ROHS 2)
- Shock: 40g's at 11ms, MIL-STD-810, Method 516.6
- Vibration: 15Hz to 2,000Hz, MIL-STD-810, Method 514.5
- Humidity: 95% R-H, MIL-STD-810, Method 507.4
- Altitude: 80,000 feet
- NAND Single Level Cell flash (SLC) or Multi Level Cell flash (MLC)
- Capacities supported: SLC: 4 - 64GB, MLC: 8 - 128GB
- Supports 3.3-Volt and 5-Volt operation
- Available in Fixed Drive or Removable configurations
- Solid State – no moving parts
- Available upon request – Custom CIS, mechanical features, labels and packaging
- Optional conformal coating for protection from moisture, salt fog, dust, etc.
- Ruggedization options for environments with extreme shock and vibration conditions

*Dependent card capacity/configuration, host configuration and testing equipment.

Delkin Devices' Ultra High Performance CompactFlash cards are manufactured in the USA at our own facilities in Poway, California. The cards are supported by Delkin's locked-down Bill of Materials that ensures consistent product performance and future compatibility. Delkin's Industrial line of CompactFlash is the perfect solution for enterprises demanding specific higher qualitative and performance functions in a widely accepted, time-tested form factor.

Applications:

- Industrial Computers
- Embedded Systems
- Data Acquisition
- Automotive
- Flight Systems
- Manufacturing
- Military
- Telecommunications
- Agriculture
- Gaming

1.1 Part Numbers

Delkin Devices' Ultra High Performance CompactFlash cards are available in the following Configurations (other capacities available upon request):

Flash Type & Operating Temp	Capacity	Part Number
SLC (-40 to +85°C)	4GB	CE04TMCVR -xx000-D
	8GB	CE08TLQVR -xx000-D
	16GB	CE16TGPVR-xx000-D
	32GB	CE32MGGYR-xx000-D
	64GB	CE64MGMYR-xx000-D
MLC (-40 to +85°C)	4GB	CE04NHUYR-xx000-D
	8GB	CE08NHUYR-xx000-D
	16GB	CE16NGTYR-xx000-D
	32GB	CE32NKBYR-xx000-D
	64GB	CE64NKOYR-xx000-D
	128GB	CE1HNKCYR-xx000-D

Notes:

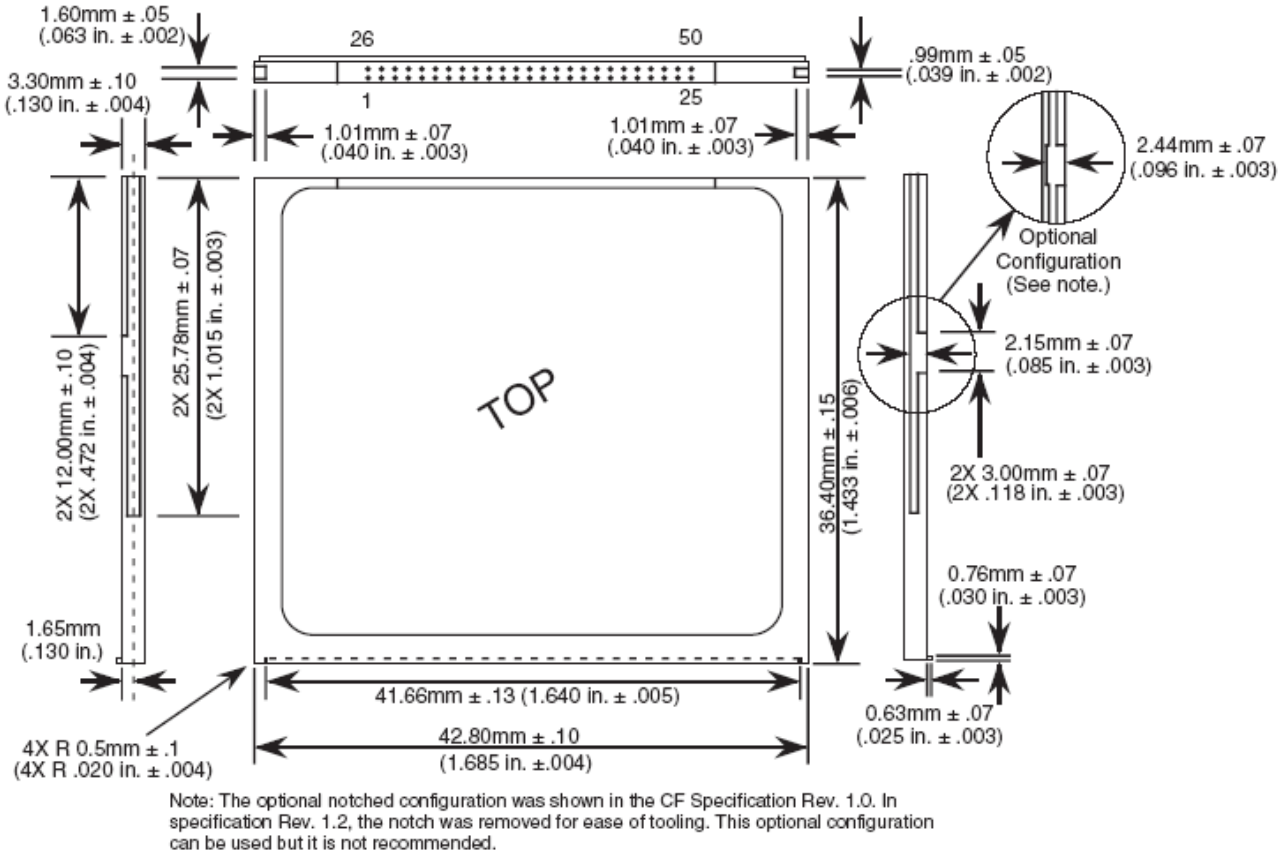
- To configure the card for removable, fixed disk, etc., replace the xx in the part numbers above as follows:
  - FD: Fixed Disk, DMA/UDMA Enabled
  - F1: Fixed Disk, DMA/UDMA Disabled
  - F2: Fixed Disk, DMA Enabled, UDMA Disabled
  - XX: Removable Disk, DMA/UDMA Enabled
  - X1: Removable Disk, DMA/UDMA Disabled
  - X2: Removable Disk, DMA Enabled, UDMA Disabled
  - X3: Removable Disk, DMA Enabled, UDMA Restricted to UDMA 2
- To add Conformal Coating, change the 000 in the part number to 0**5**0.
- To add full mechanical ruggedization (which may include underfill / epoxy on component leads, conformal coating and silicone sealant between main components and case) change the CE in the part number to CR.
- Usable capacities are within 10% of the gross capacity figures shown above, which is typical with all NAND flash devices, as a small portion of the total is needed for controller firmware and spare block reserves.

1.2 Mechanical Specifications

Delkin Devices Ultra High Performance CompactFlash cards are Type I CompactFlash cards.

1.3 Dimensions

Length:	36.4 ± 0.15 mm (1.433 ±.006 in.)
Width:	42.80 ± 0.10 mm (1.685 ±.004 in.)
Thickness Including Label Area:	3.3 mm ± 0.10 mm (.130 ± .004 in.)
Weight:	12.0 g typical



Note: The optional notched configuration was shown in the CF Specification Rev. 1.0. In specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.

Figure 1. CF Card Dimensions

2.0 Product Specifications

2.1 System Performance

Card Configuration	Sustained Read (MB/s)	Sustained Write (MB/s)
4GB SLC	95	40
8GB SLC	100	80
16GB SLC	140	105
32GB SLC	150	130
64GB SLC	150	135
4GB MLC	65	12
8GB MLC	130	25
16GB MLC	140	25
32GB MLC	150	45
64GB MLC	150	60
128GB MLC	150	70

Note: Figures reported in UDMA 7 mode, using CrystalDiskMark to benchmark performance. All values dependent on card capacity/configuration, host configuration and testing environment.

2.2 Reliability

Parameter	Value
Endurance**	64GB SLC: 57 TBW 128GB MLC: 2 TBW
MTBF***	>2 million hours at 0°C >100,000 hours at 60°C
Data Retention (at 30°C)	SLC: 10 years up to 10% of P/E cycles consumed, 1 year after 100% of P/E cycles consumed MLC: 5 Years up to 10% of P/E cycles consumed, 1 year after 100% of P/E cycles consumed
Connector Durability	10,000 insertion cycles

** Endurance estimates based on Enterprise Workload per JEDEC JESD219A. The figures provided are estimates and not guarantees of endurance. Actual results may vary depending on usage, operating temperature and other conditions. Contact Delkin for endurance estimates on other capacities.

*** Dependent on configuration and testing environment

2.3 Environmental Specifications

Features	Operating
Storage Temperature	-50 ~ 100°C
Operating Temperature	SLC Industrial: -40 ~ 85°C MLC Industrial: -40 ~ 85°C
Humidity	5% – 95% RH, non-condensing
Vibration	15Hz to 2000Hz (MIL-STD-810, Method 514.5)
Shock	40g's at 11ms
Altitude	80,000 feet max.

3.0 CF Card Interface

3.1 Card Pin Assignment

	Memory card mode		I/O card mode		True IDE mode	
Pin No.	Signal Name	I/O	Signal Name	I/O	Signal Name	I/O
1	GND	—	GND	—	GND	—
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	-CE1	I	-CE1	I	-CS0	I
8	A10	I	A10	I	A10	I
9	-OE	I	-OE	I	-ATASEL	I
10	A9	I	A9	I	A9	I
11	A8	I	A8	I	A8	I
12	A7	I	A7	I	A7	I
13	Vcc	—	Vcc	—	Vcc	—
14	A6	I	A6	I	A6	I
15	A5	I	A5	I	A5	I
16	A4	I	A4	I	A4	I
17	A3	I	A3	I	A3	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	-IOIS16	O	-IOCS16	O
25	-CD2	O	-CD2	O	-CD2	O
26	-CD1	O	-CD1	O	-CD1	O

	Memory card mode		I/O card mode		True IDE mode	
Pin No.	Signal Name	I/O	Signal Name	I/O	Signal Name	I/O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	-CE2	I	-CE2	I	-CS1	I
33	-VS1	O	-VS1	O	-VS1	O
34	-IORD	I	-IORD	I	-IORD	I
35	-IOWR	I	-IOWR	I	-IOWR	I
36	-WE	I	-WE	I	-WE	I
37	RDY/-BSY	O	-IREQ	O	INTRQ	O
38	Vcc	—	Vcc	—	Vcc	—
39	-CSEL	I	-CSEL	I	-CSEL	I
40	-VS2	O	-VS2	O	-VS2	O
41	RESET	I	RESET	I	-RESET	I
42	-WAIT	O	-WAIT	O	IORDY	O
43	-INPACK	O	-INPACK	O	DMARQ	O
44	-REG	I	-REG	I	-DMACK	I
45	BVD2	I/O	-SPKR	I/O	-DASP	I/O
46	BVD1	I/O	-STSCHG	I/O	-PDIAG	I/O
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	—	GND	—	GND	—

3.2 Card Pin Explanation

Signal Name	Direction	Pin Number	Description
A10 to A0 (PC Card Memory mode)	I	8, 10, 11, 12, 14,15, 16, 17, 18, 19, 20	Address bus is A10 to A0. A10 is MSB and A0 is LSB.
A10 to A0 (PC Card Memory mode)			
A2 to A0 (True IDE mode)		18, 19, 20	Address bus is A10 to A0. Only A2 to A0 are used, A10 to A3 should be grounded by the host.
BVD1 (PC Card Memory mode)	I/O	46	BVD1 outputs the battery voltage status in the card. This output line is constantly driven to a high state since a battery is not required for this product.
-STSCHG (PC Card I/O mode)			-STSCHG is used for changing the status of Configuration and status register in attribute area.
-PDIAG (True IDE mode)			-PDIAG is the Pass Diagnostic signal in Master/Slave handshake protocol.
BVD2 (PC Card Memory mode)	I/O	45	BVD2 outputs the battery voltage status in the card. This output line is constantly driven to a high state since a battery is not required for this product.
-SPKR (PC Card I/O mode)			-SPKR outputs speaker signals. This output line is constantly driven to a high state since this product does not support the audio function.
-DASP (True IDE mode)			-DASP is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory mode)	O	26, 25	-CD1 and -CD2 are the card detection signals. -CD1 and -CD2 are connected to ground, so host can detect that the card is inserted or not.
-CD1, -CD2 (PC Card I/O mode)			
-CD1, -CD2 (True IDE mode)			

Signal Name	Direction	Pin Number	Description
-CE1, -CE2 PC Card Memory mode) Card Enable	I	7, 32	-CE1 and -CE2 are low active card select signals. Byte/Word/Odd byte modes are defined by combination Card Enable of -CE1, -CE2 and A0.
-CE1, -CE2 (PC Card I/O mode) Card Enable			
-CS0, -CS1 (True IDE mode) Card Enable			-CE2 is used for select the Alternate Status Register and the Device Control Register while -CE1 is the chip select for the other task file registers.
-CSEL (PC Card Memory mode)	I	39	This signal is not used.
-CSEL (PC Card I/O mode)			
-CSEL (True IDE mode)			This signal is used to configure this device as a Master or a Slave when configured in the True IDE mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 to D0 (PC Card Memory mode)	I/O	31, 30, 29, 28, 27, 49, 48, 47, 6, 5, 4, 3, 2, 23, 22, 21	Data bus is D15 to D0. D0 is the LSB of the even byte of the word. D8 is the LSB of the odd byte of the word.
D15 to D0 (PC Card I/O mode)			
D15 to D0 (True IDE mode)			
GND (PC Card Memory mode)	—	1, 50	Ground
GND (PC Card I/O mode)			
GND (True IDE mode)			
-INPACK (PC Card Memory mode)	O	43	This signal is not used and should not be connected at the host.

Signal Name	Direction	Pin Number	Description
-INPACK (PC Card I/O mode) Input Acknowledge			This signal is asserted low by this card when the card is selected and responding to an I/O read cycle at the address that is on the address bus during -CE and-IORD are low. This signal is used for the input data buffer control.
DMARQ (True IDE mode)			This signal is a DMA Request that is used for DMA data transfers between host and device.
-IORD (PC Card Memory mode)	I	34	This signal is not used.
-IORD (PC Card I/O mode)			-IORD is used for control of read data in I/O task file area. This card does not respond to -IORD until I/O card interface setting up.
-IORD (True IDE mode)			-IORD is used for control of read data in I/O task file area. This card does not respond to -IORD until True IDE interface setting up.
-IOWR (PC Card Memory mode)	I	35	This signal is not used.
-IOWR (PC Card I/O mode)			-IOWR is used for control of data write in I/O task file area. This card does not respond to -IOWR until I/O card interface setting up.
-IOWR (True IDE mode)			-IOWR is used for control of data write in I/O task file area. This card does not respond to -IOWR until True IDE interface setting up.
-OE (PC Card Memory mode)	I	9	-OE is used for the control of reading register's data in attribute area or task file area.
-OE (PC Card I/O mode)			-OE is used for the control of reading register's data in attribute area.
-ATASEL (True IDE mode)			To enable True IDE mode this input should be grounded by the host.

Signal Name	Direction	Pin Number	Description
RDY/-BSY (PC Card Memory mode)	O	37	The signal is RDY/-BSY pin. RDY/-BSY pin turns low level during the card internal initialization operation at Vcc applied or reset applied, so next access to the card should be after the signal turned high level.
-IREQ (PC Card I/O mode)			This signal is active low -IREQ pin. The signal of low level indicates that the card is requesting software service to host, and high level indicates that the card is not requesting.
INTRQ (True IDE mode)			This signal is the active high Interrupt Request to the host.
-REG (PC Card Memory mode)	I	44	-REG is used during memory cycles to distinguish between task file and attribute memory accesses. Attribute memory select High for task file, Low for attribute memory is accessed.
-REG (PC Card I/O mode)			-REG is constantly low when task file or attribute memory is accessed.
-DMACK (True IDE mode)			This is a DMA Acknowledge signal by the host in response to DMARQ to initiate DMA transfers.
RESET (PC Card Memory mode)	I	41	This signal is active high RESET pin. If this signal is asserted high, the card internal initialization begins to operate. During the card internal initialization RDY/-BSY is low. After the card internal initialization RDY/-BSY is high.
RESET (PC Card I/O mode)			This signal is active high RESET pin. If this signal is asserted high, the card internal initialization begins to operate. In this mode, RDY/-BSY signal cannot be used, so using Status Register the Ready/Busy status can be confirmed.

Signal Name	Direction	Pin Number	Description
-RESET (True IDE mode)			This signal is active low -RESET pin. If this signal is asserted low, all the registers in this card are reset. In this mode, RDY/-BSY signal cannot be used, so using status register the Ready/Busy status can be confirmed.
Vcc (PC Card Memory mode)	—	13, 38	+5 V, +3.3 V power.
Vcc (PC Card I/O mode)			
Vcc (True IDE mode)			
-VS1, -VS2 (PC Card Memory mode)	O	33, 40	These signals are intended to notify Vcc requirement to host. -VS1 is held grounded and -VS2 is non-connected in this card.
-VS1, -VS2 (PC Card I/O mode)			
-VS1, -VS2 (True IDE mode)			
-WAIT (PC Card Memory mode)	O	42	This signal is active low -WAIT pin. In this card this signal is constantly high level.
-WAIT (PC Card I/O mode)			
IORDY (True IDE mode)			This output signal may be used as IORDY. In this card this signal is constantly high impedance.
-WE (PC Card Memory mode)	I	36	-WE is used for the control of writing register's data in attribute memory area or task file area.
-WE (PC Card I/O mode)			-WE is used for the control of writing register's data in attribute memory area.
-WE (True IDE mode)			This input signal is not used and should be connected to Vcc by the host.

Signal Name	Direction	Pin Number	Description
WP (PC Card Memory mode)	O	24	WP is held low because this card does not have write-protect switch.
-IOIS16 (PC Card I/O mode)			-IOIS16 is asserted when task file registers are accessed in 16-bit mode.
-IOCS16 (True IDE mode)			This output signal is asserted low when this device is expecting a word data transfer cycle.

4.0 Electrical Interface

4.1 Absolute Maximum Conditions

Parameter	Symbol	Conditions
Input Power	Vcc	-0.3V min. to 6.5V Max
Voltage on any pin except Vcc with respect to GND	V	-0.5V min. to Vcc + 0.5V Max

4.2 Power Consumption

Voltage	Read	Write	Idle
3.3V Input	380 mA max	530 mA max	1.06 mA max
5V Input	250 mA max	350 mA max	0.7 mA max

4.3 Input Leakage Current

Type	Parameter	Symbol	Conditions	Min	Typ	Max	Units
IxZ	Input Leakage Current	IL	VHI = Vcc / VIL = GND	-1		1	µA
IxU	Pull Up Resistor	RPU1	Vcc = 5.0V	50k		500k	Ohm
IxD	Pull Down Resister	RPD1	Vcc = 5.0V	50k		500k	Ohm

4.4 Input Characteristics

Type	Parameter	Symbol	Min Typ Max			Min Typ Max			Units
			Vcc = 3.3V			Vcc = 5.0V			
1	Input Voltage CMOS	Vih Vil	2.4		0.6	4.0		0.8	Volts
2	Input Voltage CMOS	Vih Vil	1.5		0.6	2.0		0.8	Volts
3	Input Voltage CMOS Schmitt Trigger	Vth Vtl		1.8 1.0			2.8 2.0		Volts

4.5 Output Drive Type

All outputs drive types are CMOS level.

4.6 Output Drive Characteristics

Type	Parameter	Symbol	Conditions	Min	Typ	Max	Units
O1	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	Vcc -0.8V		GND +0.4V	Volts
02	Output Voltage	Voh Vol	Ioh = -8 mA Iol = 8 mA	Vcc -0.8V		GND +0.4V	Volts

4.7 Interface/Bus Timing

There are two types of bus cycles and timing sequences that occur in the PCMCIA type interface, a direct mapped I/O transfer and a memory access. The two timing sequences are explained in detail in the PCMICA PC Card Standard. Delkin's CompactFlash Card conforms to the timing in that reference document.

4.8 CF-ATA Command Description

This section defines the software requirements and the format of the commands the host sends to the CompactFlash cards. Commands are issued to the CompactFlash card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register. The manner in which a command is accepted varies. These are three classes of command acceptance, all dependent on the host not issuing commands unless the CompactFlash card is not busy (BSY=0).

4.8.1 CF-ATA Command set

The following table summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the tasks file for each.

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h	-	-	-	-	D	-
1	Execute Drive Diagnostic	90h	-	-	-	-	D	-
1	Erase Sector(s)	C0h	-	Y	Y	Y	Y	Y
1	Flush Cache	E7h	-	-	-	-	D	-
2	Format Track	50h	-	Y	-	Y	Y	Y
1	Identify Device	ECh	-	-	-	-	D	-
1	Idle	E3h or 97h	-	Y	-	-	D	-
1	Idle Immediate	E1h or 95h	-	-	-	-	D	-
1	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
1	Key Management Structure Read	B9 Feature 0-127	C	C	C	C	D C	-
1	Key Management Read Keying Material	B9 Feature 80	C	C	C	C	D C	-
2	Key Management Change Key Management Value	B9 Feature 81	C	C	C	C	D C	-
1	NOP	00h	-	-	-	-	D	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read DMA	C8h	-	Y	Y	Y	Y	Y
1	Read Long Sector	22h or 23h	-	-	Y	Y	Y	Y
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y
1	Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Recalibrate	1Xh	-	-	-	-	D	-
1	Request Sense	03h	-	-	-	-	D	-
1	Security Disable Password	F6h	-	-	-	-	D	-
1	Security Erase Prepare	F3h	-	-	-	-	D	-
1	Security Erase Unit	F4h	-	-	-	-	D	-
1	Security Freeze Lock	F5h	-	-	-	-	D	-
1	Security Set Password	F1h	-	-	-	-	D	-
1	Security Unlock	F2h	-	-	-	-	D	-
1	Seek	7Xh	-	-	Y	Y	Y	Y
1	Set Features	EFh	Y	-	-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-
1	Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
1	Standby	E2h or 96h	-	-	-	-	D	-
1	Standby Immediate	E0h or 94h	-	-	-	-	D	-
1	Translate Sector	87h	-	Y	Y	Y	Y	Y
1	Wear Level	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	-	D	-
2	Write DMA	CAh	-	Y	Y	Y	Y	Y
2	Write Long Sector	32h or 33h	-	-	Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh	-	Y	Y	Y	Y	Y

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
2	Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
3	Write Verify	3Ch	-	Y	Y	Y	Y	Y

1. FR = Features Register
2. SC = Sector Count Register
3. SN = Sector Number Register
4. CY = Cylinder Register
5. DH = Card/Drive/Head Register
6. LBA = Logical Block Address Mode Supported (see command description for use).
7. Y = The register contains a valid parameter for this command.
8. For the Drive/Head Register:

    - Y – both the CompactFlash card and head parameters are used;
    - D – only the CompactFlash card parameter is valid and not the head parameter.

5.0 Comparing CF-ATA to PC Card-ATA and True IDE

This section details the differences between CF-ATA when compared to the *PC Card-ATA* and *True IDE*.

5.1 Electrical Differences

5.1.1 TTL Compatibility

CF is not TTL compatible, it is a purely CMOS interface. Refer to Electrical Specification section covered earlier in this document.

5.1.2 Pull Up Resistor Input Leakage Current

The minimum pull up input leakage current is 50K ohms rather than the 10K ohms stated in the PCMCIA specification.

5.2 Functional Differences

5.2.1 Additional Set Features Codes in CF-ATA

The following *Set Features* codes provide additional functionality in CF-ATA, but are not standard in PC Card-ATA or True IDE:

1. 69H, Accepted for backward compatibility
2. 96H, Accepted for backward compatibility
3. 97H, Accepted for backward compatibility
4. 9AH, Set the host current source capability

5.2.2 Additional Commands in CF-ATA

The following commands provide additional functionality in CF-ATA, but are not standard PC Card-ATA commands.

PC Card-ATA and True IDE define the following command codes as *vendor unique*:

1. C0H, Erase Sectors
2. 87H, Translate Sector
3. F5H, Wear Level

PC Card-ATA and True IDE define the following command codes as *reserved*:

1. 03H, Request Sense
2. 38H, Write Without Erase
3. CDH, Write Multiple Without Erase

5.2.3 Idle Timer

The CF-ATA Idle timer uses an increment value of 5 ms, rather than the 5 second minimum increment value specified in PC Card-ATA/True IDE.

5.2.4 Recovery from Sleep Mode

For CF devices, recovery from sleep mode is accomplished by issuing another command to the device. A hardware or software reset is not required.

6.0 SMART Feature Set

Delkin Devices Ultra High Performance CF cards support the SMART command set and defines some vendor-specific data to report spare/bad block numbers in each memory management unit.

Value	Command	Value	Command
D0h	Read Data	D5h	Reserved
D1h	Read Attribute Threshold	D6h	Reserved
D2h	Enable / Disable Autosave	D8h	Enable SMART Operations
D3h	Save Attribute Values	D9h	Disable SMART Operations
D4h	Execute OFF-LINE Immediate	DAh	Return Status

If the reserved size is below the threshold, the status can be read from the Cylinder Register using the Return Status command (DAh.)

6.1 SMART Data Structure

The following 512 bytes make up the device SMART data structure. Users can obtain the data using the “Read Data” command (D0h.)

Byte	F / V	Description
0 – 1	X	Revision code
2 – 361	X	Vendor specific (see Section 6.2 for details)
362	V	Off-line data collection status
363	X	Self-test execution status byte
364 – 365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368 – 369	F	SMART capability
370	F	Error logging capability • 7-1 Reserved • 0 1= Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375 – 385	R	Reserved
386 – 395	F	Firmware Revision / Date Code
396 – 399	R	Reserved
400 – 406	F	Controller
407 – 511	X	Reserved

Notes:

1. F = content (byte) is fixed and does not change
2. V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device
3. X = content (byte) is vendor specific and may be fixed or variable
4. R = content (byte) is reserved and shall be zero.

6.2 SMART Attributes

The following table defines the vendor specific data in byte 2 to 361 of the 512-byte SMART data structure.

Attribute ID (hex)	Raw Attribute Value						Attribute Name
01	LSB	MSB	00	00	00	00	Read error rate
05	LSB	MSB	00	00	00	00	Reallocated sector count
0C	LSB	MSB	00	00	00	00	Power cycle count
A1	LSB	MSB	00	00	00	00	Number of valid spare blocks
A2	LSB	MSB	00	00	00	00	Number of child pairs
A3	LSB	MSB	00	00	00	00	Number of initial invalid blocks
A4	LSB			MSB	00	00	Number of total erase count
A5	LSB			MSB	00	00	Maximum erase count
A6	LSB			MSB	00	00	Minimum erase count
A7	LSB			MSB	00	00	Average erase count
C0	LSB			MSB	00	00	Power-off retract count
C7	LSB	MSB	00	00	00	00	UDMA CRC error count
F1	LSB					MSB	Total LBAs written (each write unit = 32MB)
F2	LSB					MSB	Total LBAs read (each read unit = 32MB)